AMENDMENTS TO THE SPECIFICATION:

Please replace paragraph [0002] of the specification as filed with the following:

[0002] As illustrated in the equivalent circuit diagram depicted in FIGURE ~~5~~ 4, integrated circuit comparators typically include: a bias system generating a defined current bias to each transistor; an input differential pair--either complementary metal oxide semiconductor (CMOS) or bipolar junction transistors--that, for a given overdrive voltage V(ov)=(V(inp)-V(inn)) generate a differential current given by I(ov)=gm*V(ov), where gm is the transconductance of the input differential pair at the steady-state operating point V(ov)=0 volts (V); a gain stage node ngain converting the current I(ov) to (in the CMOS case) a voltage gain and having a transition speed depending on the overdrive current I(ov) available, the voltage excursion required between the high and low levels at the ngain node, and the capacitive load at the ngain node, including any Miller capacitance from the comparator's output stage; and a gain stage assuring a given slew rate at the comparator output out.

Please replace paragraph [0012] of the specification as filed with the following:

[0012] FIGURE 3 is a block diagram of a low power integrated circuit pulse generator and comparator according to one embodiment of the present invention; and

Please delete paragraph [0013] of the specification as filed.

Please replace paragraph [0014] of the specification as filed with the following:

[0014] FIGURE ~~5~~ 4 is an equivalent circuit diagram of a typical integrated circuit comparator.

Please delete paragraph [0033] of the specification as filed.

Please cancel Figures 4A and 4B of the application as filed, and relabel Figure 5 as filed to Figure 4.